In the Specification:

Please amend the paragraph on page 17, line 5 to page 18, line 2 of the specification to read as follows:

The power source switchover circuitry 103 contains start-up circuitry 200 coupled to the VCCEXT line 106 and current mirror circuitry 205. The current mirror circuitry is coupled to the ~~gate~~ base of the transistor 210, which has its collector connected to the VCCSUB line 108 and its emitter connected to a resistor 215. The other terminal of the resistor is connected to a gate of a P-channel transistor 220. The line connecting the resistor 215 and the gate of the P-channel transistor 220 provides the VREF signal 104. The source of the P-channel transistor 220 is coupled to VCCEXT 106 and the drain is coupled to the gates of twoN-channel transistors 225 and 226, which have their source terminals connected to VSS 110. Coupled between the source terminal of the P-channel transistor 220 and the drain channel of the N-channel transistor 226 are a series of resistors, RA, R1-R6, and RB, which form a voltage divider. A node coupled between the R3 and the R4 resistor provides the VA3 signal 105. In parallel to each of the resistors R1-R6 are fuses f1-f6, respectively, that are used to adjust or trim the value of the voltage divider, which generates the VA3 signal 103.

Please amend the paragraph on page 18, line 3 to page 19, line 3 of the specification to read as follows:

When ramping-up the primary power source, the VCCEXT signal 106 provides a boost to the startup circuitry, which causes the current mirror circuitry 205 to operate. Upon the ~~gate~~ base terminal receiving current flow, the transistor 210 will begin to lower the impedance across its collector and emitter terminals and a voltage level is developed at the VREF node 104. Simultaneously, a voltage is developed at the VA3 node 105 as dictated by the voltage divider from the resistors RA, R1-R6, and RB taking into account the status of fuses f1-f6. At the trip point, the voltage level of the VREF signal 104 and the VA3 signal 105 cross as the VREF signal 104 has a steeper slope than the VA3 signal 105. The trip point for the power source switchover circuitry 103 and is generally set for 2.5volts. It should be noted that during the time that the monitor and switchover circuitry 101 is powered on the secondary power source, such as a battery, the substrate is at the level of the secondary power source, such as 3V. When the substrate is powered by the secondary power source at 3V, all of the P-channel transistors are in a weak inversion state (i.e., back bias mode) until the switchover from the secondary to the primary power source occurs and the voltage potential of the substrate drops to the supply level of the primary power source.